CLAIMS

1. A layer structure comprising :

a semi-conductor heterostructure;

at least one metallic interlayer deposited next to at least one surface and in at least one region of said heterostructure; and

a dielectric layer coated next to said interlayer.

2. A layer structure according to claim 1 wherein only one surface is deposited with said metallic interlayer.

3. A layer structure according to claim 1 wherein only the top surface is deposited with said metallic interlayer.

4. A layer structure according to claim 1 further comprising an oxide layer between said heterostructure and said interlayer.

5. A layer structure according to claim 2 further comprising an oxide layer between said heterostructure and said interlayer.

6. A layer structure according to claim 2 wherein said heterostructure is a single quantum well structure, and multiple quantum well structure, a superlattice structure or a quantum dot structure.

7. A layer structure according to claim 2 wherein said heterostructure comprises

a AlGaAs/GaAs quantum well structure having a plurality of alternating AlGaAs and GaAs layers; or

an InGaAs/GaAs quantum well structure having a plurality of alternating InGaAs and GaAs layers.

8. A layer structure according to claim 2 wherein said interlayer comprises a single layer of metal, a single layer of alloyed metal, multiple layers of metal, multiple layers of alloyed metal, or multiple layers of metal and alloyed metal.

9. A layer structure according to claim 2 wherein said interlayer is 1 to 10,000 angstrom thick.

10. A layer structure according to claim 2 wherein said interlayer is 10 to 500 angstrom thick.

11. A layer structure according to claim 2 wherein a plurality of interlayers are deposited in different regions of said heterostructure.

12. A layer structure according to claim 2 wherein a plurality of interlayers are deposited in different regions of said heterostructure, and at least two of said interlayers have different thicknesses.

13. A layer structure according to claim 2 wherein said dielectric layer is made from silica oxide or silica.

14. A layer structure according to claim 5 wherein said heterostructure is a single quantum well structure, and multiple quantum well structure, a superlattice structure or a quantum dot structure.

15. A layer structure according to claim 5 wherein said heterostructure comprises

a AlGaAs/GaAs quantum well structure having a plurality of alternating AlGaAs and GaAs layers; or

an InGaAs/GaAs quantum well structure having a plurality of alternating InGaAs and GaAs layers.

16. A layer structure according to claim 5 wherein said interlayer comprises a single layer of metal, a single layer of alloyed metal, multiple layers of metal, multiple layers of alloyed metal, or multiple layers of metal and alloyed metal.

17. A layer structure according to claim 5 wherein said interlayer is 1 to 10,000 angstrom thick.

18. A layer structure according to claim 5 wherein said interlayer is 10 to 500 angstrom thick.

19. A layer structure according to claim 5 wherein a plurality of interlayers are deposited in different regions of said heterostructure.

20. A layer structure according to claim 5 wherein a plurality of interlayers are deposited in different regions of said heterostructure, and at least two of said interlayers have different thicknesses.

21. A layer structure according to claim 5 wherein said heterostructure is made from elements from column III to V of the periodic table of elements.

22. A layer structure according to claim 5 wherein said dielectric layer is made from silica oxide or silica.

O

23. A method of post-growth tuning of an optical bandgap of a semiconductor heterostructure comprising :

forming an oxide layer on the top-surface of said heterostructure;

depositing at least one metallic interlayer on at least one region of said oxide layer; and

post-annealing said dielectric layer onto said heterostructure.

24. A method according to claim 23 wherein said oxide layer is formed by

heating said heterostructure in the presence of pure oxygen;

heating said heterostructure in the presence of oxygen and at least one inert gas;

heating said heterostructure in the presence of water-saturated pure oxygen;

heating said heterostructure in the presence of water-saturated oxygen and inert gas;

heating said heterostructure in the presence of H_2O_2-saturated pure oxygen;

heating said heterostructure in the presence of H_2O_2-saturated oxygen and inert gas; or

heating said heterostructure in the presence of H_2O_2-saturated inert gas.

25. A method of post-growth tuning of an optical bandgap of a semiconductor heterostructure comprising :

O

a) forming an oxide layer on the top-surface of said heterostructure;

b) masking said heterostructure with a mask of a predetermined pattern such that said heterostructure is exposed in unmasked regions;

c) depositing at least one metallic interlayer on said unmasked regions;

d) lifting-off said mask;

e) post-annealing said dielectric layer onto said heterostructure.

26. A method according to claim 25 wherein steps (c) and (d) are repeated to produce additional interlayers according to additional specific patterns.

27. A layer structure comprising :

a semi-conductor heterostructure;

at least one oxide layer formed on at least one surface of said heterostructure; and

a dielectric layer coated next to said oxide layer.

28. A layer structure according to claim 27 wherein said oxide layer is formed by the oxidation of said surface of said heterostructure.

O